

SoftRock v6 Exciter Builder's Notes

October 5, 2006

Be sure to use a grounded tip soldering iron in building the v6 SoftRock Exciter QSD and PA circuit boards. The soldering iron needs to have a small tip, (0.05 - 0.1 inch diameter), and be in the power range of 15 to 20 watts. A 2% silver-bearing solder with diameter of 0.015 inches works well for SMT work.

The schematic diagram, BOM (bill of materials) and board information file for the v6 SoftRock Exciter QSE and PA boards may be down loaded from the from the files area of the Yahoo SoftRock-40 group website. These pdf files will be needed during the build of the exciter kit pair.

Modification to v6 SoftRock for use with the exciter QSD and PA boards

A v6 SoftRock 40m/80m board, either a v6.0 or v6.1, is required for the exciter QSD board to operate properly since the clock signal on the SoftRock header JP1 is also the clock source for the QSD circuit on the QSD board. The SoftRock board will be the bottom board in the stack of three boards consisting of a v6 SoftRock receiver, a v6 QSE board and a v6 PA board. Properly aligned header pins need to be installed on the SoftRock board at the JP1, JP2, DC power in, and antenna locations on the board. Proper alignment of these header pin is accomplished by use of the QSE board and board stack hardware as a last construction step of the QSE board.

Construction of the QSE board

Documents required to construct the QSE board are the schematic diagram, the bill of materials and the QSE board map. The QSE board is a small board with many components and requires care in soldering components in place to prevent solder bridges. In some cases the component designators could not be included on the board and such component locations are identified on the QSE board map pdf file.

The first step of construction is to mount most of the SMT components. All SMT capacitor locations on the top and bottom of the QSE board are to be filled with 0.1 uF 1206 size capacitors. Tack one end of each capacitor to a pad and properly position the capacitor with the tip of the soldering iron and a toothpick. When the capacitor is properly positioned on its pads, solder the other end with enough solder to make a small fillet between the end of the capacitor and the pad. Reheat the first end of the capacitor and add a little solder if necessary to make a small fillet at the tacked down end of the capacitor. Excess solder may be removed with solder wick. The SOIC integrated circuits are such that if they have the same pin count as a mounting location then they are the right part for that location. The silkscreen on the top of the board shows the orientation of U1. U2 through U5 which are mounted on the bottom of the

board have their pin 1 corners identified by a small "1" marks in the bottom side copper. U1 should be mounted along with the SMT capacitors and U2 through U5 should be mounted near the end of the board construction phase to minimize static discharge exposure to the parts.

Resistors are mounted on the board in a hairpin fashion with the body of each resistor located over its silkscreen circle. The other lead of each resistor goes to the hole that is pointed to by the small radial line on the silkscreen resistor pattern. Mount the resistors with the body of each resistor lightly snugged to the board. If resistors near the corners of the board are first mounted, the mounted resistors form legs to hold the board level when soldering on the bottom of the board.

Mount all resistors, ceramic capacitors and diodes with reference to the board map to help find the component locations. Diodes D3 and D4 are each two diodes in series with the series connection above the board to form a hairpin of the two diodes. Lightly twist the two diode leads together, (banded end to unbanded end), and solder the twisted leads before the diode pair are used at the D3 or D4 location.

Electrolytic capacitors are all of the same value and no designators are shown on the board or on the board map. Make sure each capacitor is oriented with its + lead at the + hole on the electrolytic capacitor silkscreen marking.

After all resistors, capacitors and diodes are mounted to the board, the transistors and U6 may be mounted. Use the body shape silk screen marking to help in proper placement of each of the transistors and U6. U2 through U5 can then be mounted on the bottom of the board.

Do a careful visual check of soldering to make sure all component leads are properly soldered, all IC SMT pins are soldered properly, and that there are no solder bridges between pads or IC pins. Check for proper orientation of diodes and electrolytic capacitors. Measure the resistance from the DC power in pad to circuit ground and the 5 VDC line to circuit ground and make sure each resistance is greater than 1k.

Header pin groups P5, P6 and P7 should not be mounted until the PA board is built to insure proper alignment between the connectors on the two boards. Header sockets P1 through P4 may be mounted at this time if the SoftRock board is built and ready to include in the board stack. To mate the SoftRock and QSE board plug the short end of each header pin group fully into the appropriate sockets and place these connector groups between the two boards in the SoftRock locations JP1, JP2, DC power, and antenna. The header pin portion of each group should be associated with the SoftRock board. Mounting hardware should be used to align the two board and to provide proper spacing between the two boards with separation of a nylon washer, a 3/8 inch threaded spacer and a nylon washer at each corner between the two boards. Lightly tighten the board mounting hardware and check to see that the board alignment is good and that mated connector groups are properly situated between the two boards

with sockets to the bottom side of the QSE board. Solder the header sockets in place from the top side of the QSE board and header pins are soldered from the bottom side of the SoftRock board. Cut off excess lead length from the bottom side of the SoftRock board.

The clock divide ratio should be set for 40m operation by bridging pins 1 and 2 of JP1 on the bottom side of the SoftRock board.

The only external cable connected to the SoftRock board should be a stereo audio cable connected to the line-in holes on the SoftRock board. External cables to the QSE board should include a stereo audio cable connected to the line-out holes, DC power input (2 leads), antenna coax, and PTT-in.

Initial testing of the QSE board

Some initial testing may be done at this time if the external cables are connected to the two boards and the SoftRock and QSE boards are plugged together. Connect a current limited 12 VDC supply to the DC power-in leads of the QSE board and make sure supply current is less than 65 mA. (If supply current is above 65 mA, disconnect the supply and look for shorts or component orientation problems on each of the boards.) Check the 5 volt regulated supplies on both the SoftRock board and the QSE board by probing at a power pin on any of the IC devices on the boards. Check for 12 VDC at pin 1 on the QSE board P6 location. P6 pin 3 should be at zero volts with the PTT-in wire at zero volts, (or open circuited) and should rise to about 12 volts if the PTT -in wire is touched to the P6 pin 1, (12 volts). Also when the PTT-in wire is touched to 12 volts, SoftRock JP2 pin 1 should go to 5 volts which is associated with receiver mute.

SoftRock receiver operation in combination with the QSE board may be tested by first temporarily bridging between holes 1 and 3 of the P7 connector position of the QSE board. With DC power applied to the board-stack and the line-in and antenna connections made, the SoftRock should be receiving signals on 40m band when used with a program such as Rocky. When the PTT-in wire goes to 12 volts the SoftRock should go to receiver mute. If the SoftRock JP2 pins are temporarily shorted together with the PTT-in line still connected to 12 volts, the receiver should start operating again but receive no signals since the QSE antenna switch, (Q3 on the QSE board), is open.

A quadrature audio source can be used for initial testing of the QSE board QSE functions. Quadrature audio can be provided from a PC soundcard line-out if a program such as IQ GEN by DL6IAK is installed on the PC. (Please see

<http://dl6iak.ba-karlsruhe.de/projects/2001-04-28.htm>

to download the IQ GEN program program.)

With 2 kHz quadrature audio input to the line-out audio cable of the QSE board, check

for DC offset 2 kHz signals at capacitors C9, C13, C18 and C20. The DC value at these capacitors should be about 2.5 volts and the AC component will be variable and equal to the amplitude of the audio input at the line-out connections on the QSE board. Pin 2 of P5 should be at about 1.6 volts DC and pins 1 and 3 of P5 should show a somewhat ragged signal with a 40m component when viewed with a scope.

Construction of the PA board

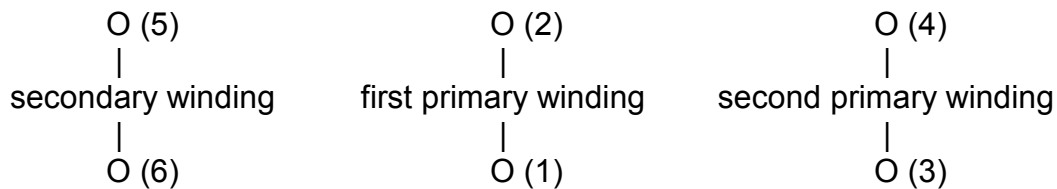
Documents required to construct the PA board are the schematic diagram, the bill of materials and the PA board map. The PA board is a small board with many components and requires care in soldering components in place to prevent solder bridges. In some cases the component designators could not be included on the board and such component locations are identified on the PA board map pdf file.

Do not mount the connectors on this board until the last step when the board is to be mated to the QSE board. Mount all other components on the board before mounting transistors Q1 and Q2.

All SMT 1206 locations on the PA board are to be filled with 0.1 uF 1206 capacitors. All electrolytic capacitors on the PA board at 10 uF. Be sure to orient each of the electrolytic capacitors with its + lead to the + hole of the silkscreen marking on the board. (The top-left capacitor has the opposite orientation of the rest of the capacitors along the left edge of the board.) Resistors and RFC1 are mounted in a hairpin fashion with the bodies of the parts lightly snugged down to the board. On the prototype PA board the components are very close together and it is advisable to mount some of the ceramic capacitors on the bottom side of the board with their bodies flat against the bottom of the board.

Pot R7 is the bias adjustment for the output power amplifier transistor Q2. The pot is not wired correctly on the board and CW rotation of the pot results in decreasing Q2 idle current. (Initially set R7 fully CW before PA board testing.)

Transformer T1 is wound with its secondary winding first wound and then the two primary windings wound bifilar on top of the secondary winding. T1 is mounted vertically on the board just above connector P1 location. Wires coming out of one side of the core go to the three holes away from P1 and wires coming out of the other side of the core go to the three holes closest to P1. The diagram below shows the wiring to the six holes associated with the T1 mounting position.



Transformer T2 is wound on a binocular core with two leads coming out of each hole on the same face of the core. T2 is mounted vertically with the leads toward the board and going to the nearest hole as shown by the mounting diagram of below.

O-----first winding-----O

O—second winding—O

All inductors, L1 through L5, are mounted vertically or slightly leaning away from other surrounding components. RFC2 is wound on a binocular core and also mounted vertically but pushed toward the top edge of the board to give room for L3.

The heat sinks for Q1 and Q2 should be carefully pressed onto the transistor cases before the transistors are mounted on the board. A little planning is needed with the heat sink of Q2 so that when Q2 is mounted to the board the horizontal portion of its heat sink will go crosswise along the short dimension of the PA board. Q1 with its heat sink in place is soldered in place slightly raised above the board so that its heat sink clears other components. Q2 is next soldered in place again making sure its heat sink clears other components. The body of diode D1 will be against the Q2 heat sink for Q2 idle current compensation for transistor heating.

The connectors between the QSE board and the PA board may now be aligned and soldered in place. Again plug the connector pairs together with the short header pins fully inserted into the sockets for the three connector pairs. Place the connector pairs between the QSE and PA boards with the sockets toward the PA board. Use the board stack hardware to help with board alignment with the board spacing set by a nylon washer, a 3/8 threaded spacer and a nylon washer providing separation distance between the two boards. With the connectors properly aligned between the two boards solder the header pins from the bottom side of the QSE board and the header sockets from the top side of the PA board. Cut off excess header pin lead length.

Initial testing of the PA board includes checking to make sure the 12 VDC power traces are not shorted to circuit ground and that the switched 12 volt signals on pin 3 of P2 is not shorted to circuit ground.

With the three v6 boards plugged together connect the antenna coax from the QSE board to a 50 ohm dummy load, connect the line-out audio cable to a PC's soundcard line-out jack, and connect the DC power leads to a current limited 12 volt DC source. Turn on DC power and make sure the supply current is less than 65 mA.

Set the PA output transistor idle current by first setting pot R6 to fully CW. Connect the PTT-in lead from the QSE board to 12 volts and note the increase in supply current.

Adjust R6 until the supply current increases by about 50 mA above the supply current first measured with the PTT-in lead grounded or floating.

Set in a frequency of about 5 kHz in the IQ Gen program and gradually increase the amplitude of the quadrature line-out signals to the QSE board. Note the increase in the supply current as the PA develops RF output to the dummy load. Observe the waveform on the dummy load to be a nice sine wave and monitor the RF output on a nearby receiver to be a single tone either above or below the center frequency by 5 kHz. Observe that the opposite sideband signal is at least 30 dB lower in amplitude than the desired output signal. Change frequency of the IQ Gen to see if RF output up to 20 kHz each side of the center frequency can be generated and that the RF output level can be set to at least 500 mW by the amplitude control on IQ Gen.

Please post any problems found in the building or testing of the QSE and PA boards on the SoftRock-40 Yahoo Group website.

Thanks and 73,
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